stopper layer as a mask to form a trench;

(C) forming a trench oxide film over a surface of the substrate that forms the trench;

(D) forming an insulating layer that fills the trench over an entire surface of the substrate;

(E) polishing the insulating layer by a chemical-mechanical polishing;

(F) removing the polishing stopper layer; and

(G) etching a part of the insulating layer to form a trench insulating layer,

wherein the method further includes the step (a) of forming an etching stopper layer for the trench oxide film over at least a portion of the trench oxide film, and wherein, in the step (G), the etching stopper layer is more resistant to the etching than the insulating layer.

Please add new claims 27-35 as follows:

--27. (new) A method as in claim 1, comprising forming the polishing stopper layer from at least two layers selected from the group consisting of a silicon nitride layer, a polycrystal silicon layer, and an amorphous silicon layer.

28. (new) A method as in claim 1, further comprising forming the trench so that an angle at an intersection between the lower surface of the trench and a side surface of the trench is greater than 90 degrees.

29. (new) A method for manufacturing a semiconductor device, comprising:

forming a trench comprising a lower surface and side surfaces in a substrate comprising silicon;

forming a trench oxide layer covering the lower surface and side surfaces;

forming rounded corner regions at an intersection of an upper surface of the substrate and the side surfaces of the trench;

forming an etch stop layer in direct contact with the trench oxide layer on the lower surface and side surfaces;

filling the trench with an insulating layer directly contacting the etch stop layer, wherein the insulating layer overfills the trench and a portion of the insulation layer extends over the upper surface of the substrate; and

etching the insulating layer using an etchant that selectively etches the etch stop layer at a rate that is slower than that of the insulating layer.

30. (new) A method as in claim 29, further comprising forming the trench so that an angle at an intersection between the lower surface of the trench and a side surface of the trench is greater than 90 degrees.

31. (new) A method as in claim 29, wherein the etching the insulating layer is carried out so that a first portion of the insulating layer that extends over the upper surface of the substrate is removed and a second portion of the insulating layer over the trench extends to a level above that of the upper surface of the substrate.

32. (new) A method as in claim 31, further comprising, after the etching the insulating layer;

implanting an impurity into a first region of the substrate;

implanting an impurity into a second region of the substrate; and

after the implanting the impurity into the second region, etching the second portion of the insulating layer, wherein the etching is controlled so that the second portion of the insulating layer extends to a level above that of the upper surface of the substrate.

33. (new) A method as in claim 31, further comprising:

forming an oxide layer on the upper surface of the substrate after the etching the insulating layer;

implanting an impurity into a first region of the substrate;

implanting an impurity into a second region of the substrate; and

after the implanting the impurity into the second region, etching the second portion of the insulating layer and the oxide layer, wherein the etching is controlled so that oxide layer is removed and the second portion of the insulating extends to a level above that of the upper surface of the substrate.

34. (new) A method for manufacturing a semiconductor device, comprising:

forming a pad insulating layer on a silicon substrate;

forming a polishing stopper layer on the pad layer;

forming a first resist layer having a specified pattern on the polishing stopper layer

etching the polishing stopper layer and the pad insulating layer using the first resist layer as a mask to yield a remaining polishing stopper layer and remaining pad insulation layer;

removing the first resist layer;

etching the silicon substrate using the remaining polishing stopper layer and remaining pad insulation layer as a mask, to form a trench in the silicon substrate;

oxidizing surfaces in the trench;

forming a silicon nitride layer on the oxidized surfaces in the trench;

forming a insulating layer on the silicon nitride layer and overfilling the trench;

planarizing the insulating layer that overfills the trench until the polishing stopper layer is reached;

removing the remaining polishing stopper layer;

etching the remaining pad insulation layer and the insulating layer so that a portion of the insulating layer extends to a level higher than that of the silicon substrate; and

performing at least one ion implantation while the insulation layer extends to a level higher than that of the silicon substrate.

35. (new) A method as in claim 34, further comprising forming the trench so that an angle at an intersection between the lower surface of the trench and a side surface of the trench is greater than 90 degrees.--

IN THE DRAWINGS:

In Figs. 34-38, please insert the terms --Prior Art-- as indicated in red on the attached sheets.